Doc. Number:

■ Tentative Specification
☐ Preliminary Specification
☐ Approval Specification

MODEL NO.: N133HSE
SUFFIX: DA1

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

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REVISION HISTORY

Version	Date	Page	Description
1.0	6.Dec, 2012	All	Tentative spec. Ver.1.0 was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N133HSE – DA1 is a 13.3” TFT Liquid Crystal Display module with 30 pins eDP interface. This product supports 1920 x 1080 FHD model and can display 16,777,216 colors. The Backlight unit is not built in.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	13.3 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.1529 (H) x 0.1529 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8 bit)	color	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Power Consumption	cell 1.24W(Max.)	(1)	

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

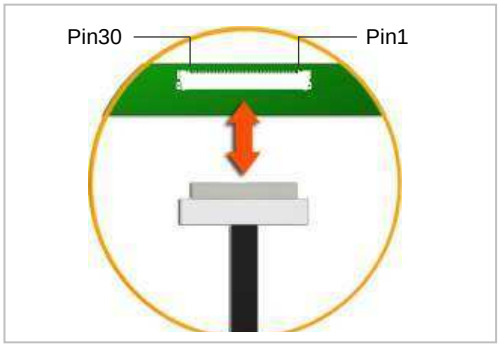
2. MECHANICAL SPECIFICATIONS

item		Min.	Typ.	Max.	Unit	Note
Size	Horizontal (H) with PCB	301.82	301.97	302.12	mm	(1) (2)
	Vertical (V) with PCB	185.66	186.16	186.66	mm	
	Vertical (V) w/o PCB	175.04	175.19	175.34	mm	
	Thickness (T) with PCB	-	1.9	-	mm	
	Thickness (T) w/o PCB	-	1.07	-	mm	
Weight (with polarizer release paper)		-	126	140	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12

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User's connector Part No: IPEX-20453-030T-01

2.1.2 LED Light-Bar Connector

Connector Part No.: STM MSK24022P10A

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

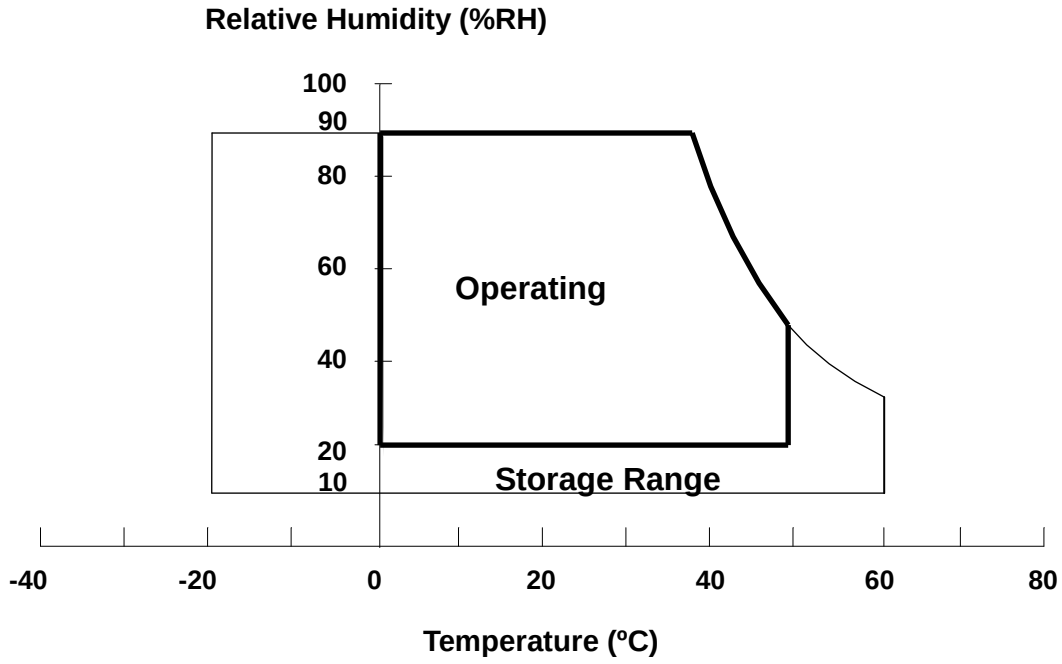
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



3.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

High temperature or humidity may reduce the performance of panel. Please store LCD panel within the specified storage conditions.

Storage Condition: With packing.

Storage temperature range: 25±5 ºC.

Storage humidity range: 50±10%RH.

Shelf life: 30days

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3.3 ELECTRICAL ABSOLUTE RATINGS(OPEN CELL)

3.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	25	V	
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	
Converter Control Signal Voltage	LED_EN	-0.3	5	V	

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

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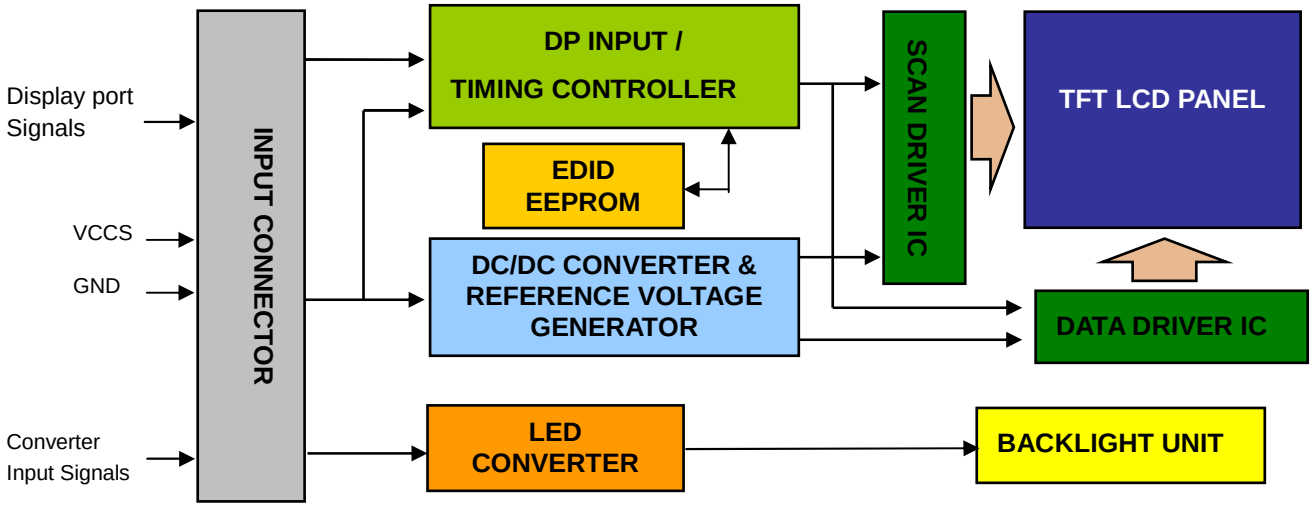
4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

4.2.1 PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for CMI test)	
2	H_GND	High Speed Ground	
3	ML1-	Complement Signal-Lane 1	
4	ML1+	True Signal-Main Lane 1	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for CMI test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	

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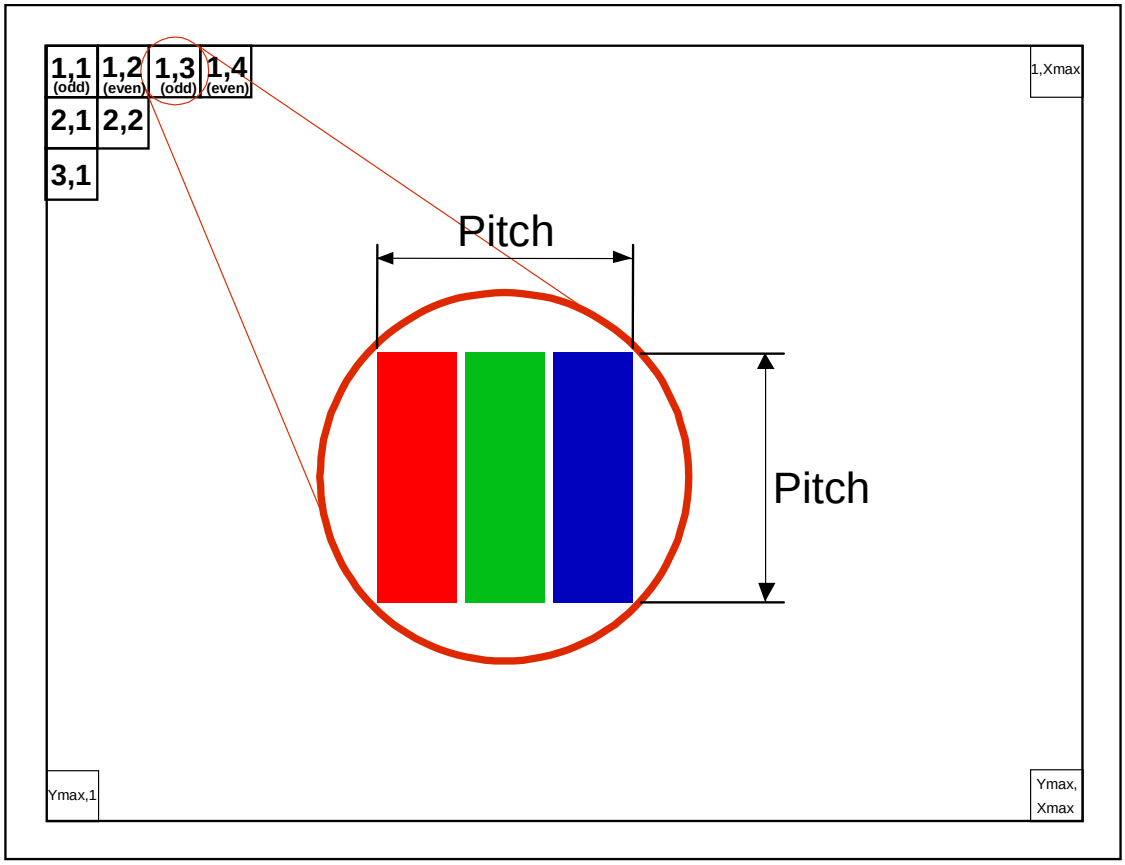
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for CMI test)	
25	NC	No Connection (Reserved for CMI test)	
26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for CMI test)	

Note (1) The first pixel is odd as shown in the following figure.



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4.2.3 LED CONVERTER OUTPUT PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	VLED Output	LED driver output	
2	VLED Output	LED driver output	
3	NC	No Connection (Reserve)	
4	LED_CA1	LED Cathode 1	
5	LED_CA2	LED Cathode 2	
6	LED_CA3	LED Cathode 3	
7	LED_CA4	LED Cathode 4	
8	LED_CA5	LED Cathode 5	
9	LED_CA6	LED Cathode 6	
10	NC	No Connection (Reserve)	

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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

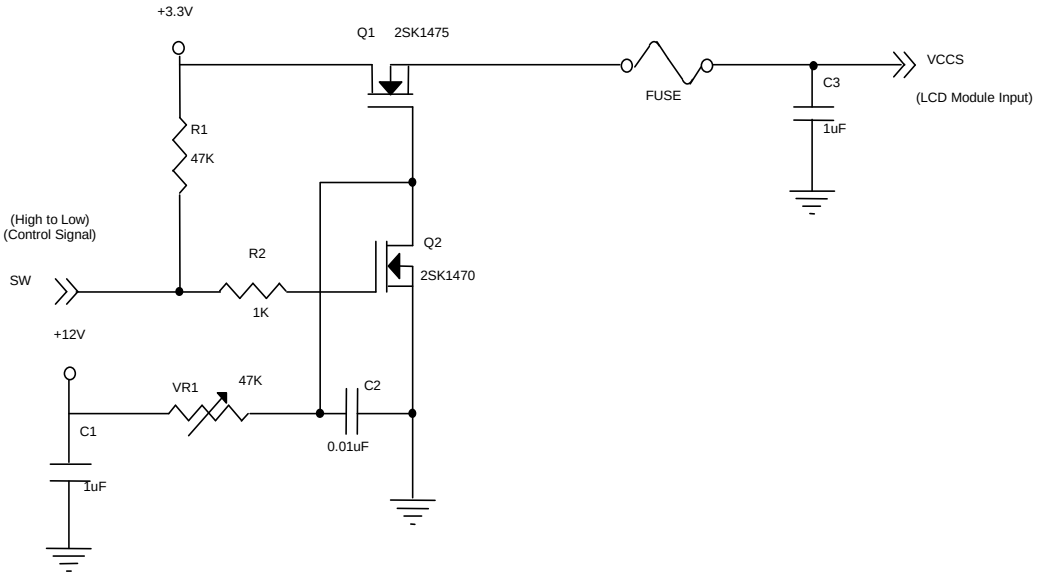
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
HPD	High Level		3.0	-	3.6	V	
	Low Level		0	-	0.4	V	
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc		315	375	mA	(3)a
	White			352	412	mA	(3)b

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

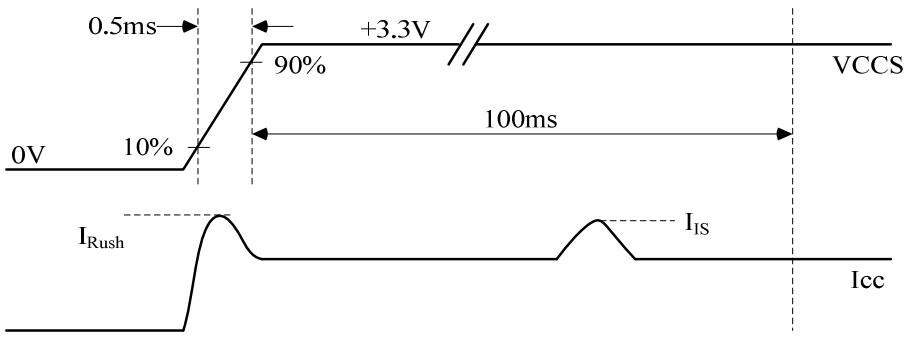
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms



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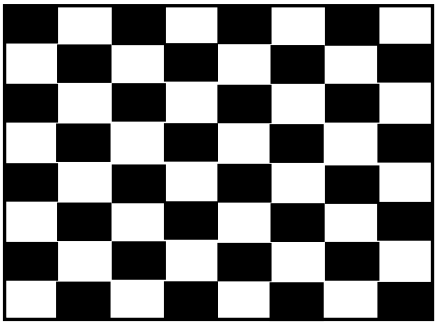
Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. White Pattern

Active Area

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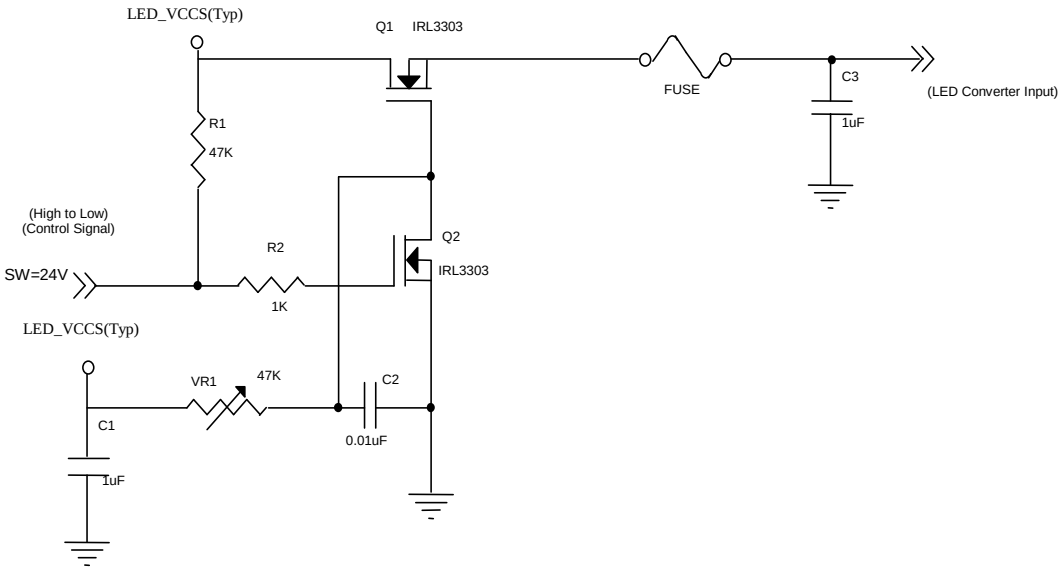
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	7.0	12.0	21.0	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.3	-	5.0	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	PWM High Level		2.3	-	5.0	V	
	PWM Low Level		0	-	0.5	V	
PWM Control Duty Ratio			5	-	100	%	(2)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(3)
LED Power Current	LED_VCCS =Typ.	ILED	293	329	429	mA	(4)

Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms

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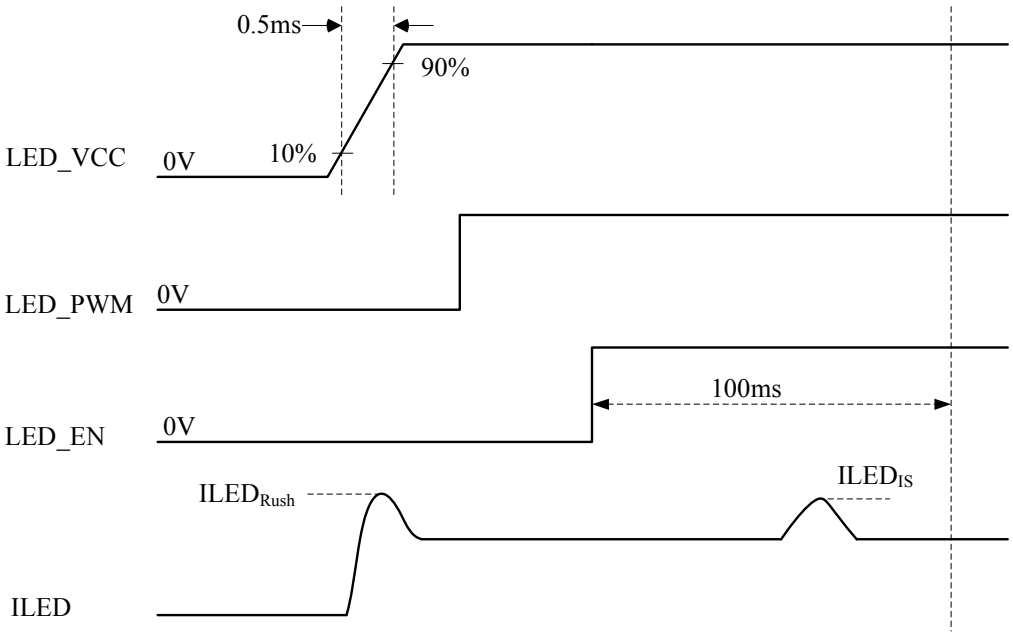

Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (4) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

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4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

4.4.1 DISPLAY PORT INTERFACE

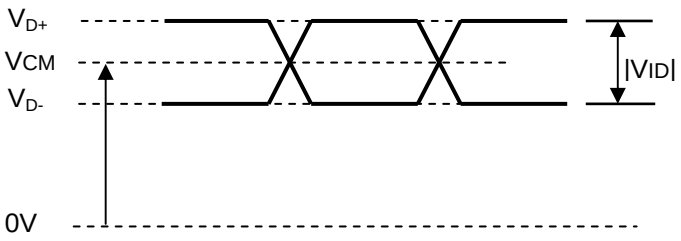
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(3)
AUX AC Coupling Capacitor	C_{AUX}	75		200	nF	(2)

Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.1.

(2) The AUX AC Coupling Capacitor should be placed on Source Devices.

(3)The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

Single Ended



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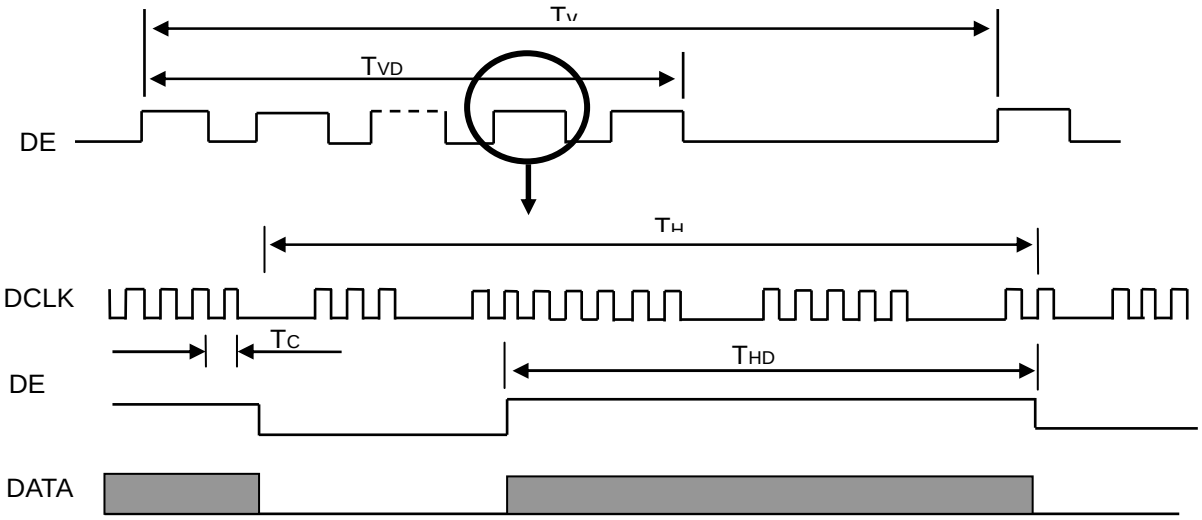
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	116.17	138.78	142.77	MHz	-
DE	Vertical Total Time	TV	1103	1112	1462	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	32	TV-TVD	TH	-
	Horizontal Total Time	TH	2058	2080	2910	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM



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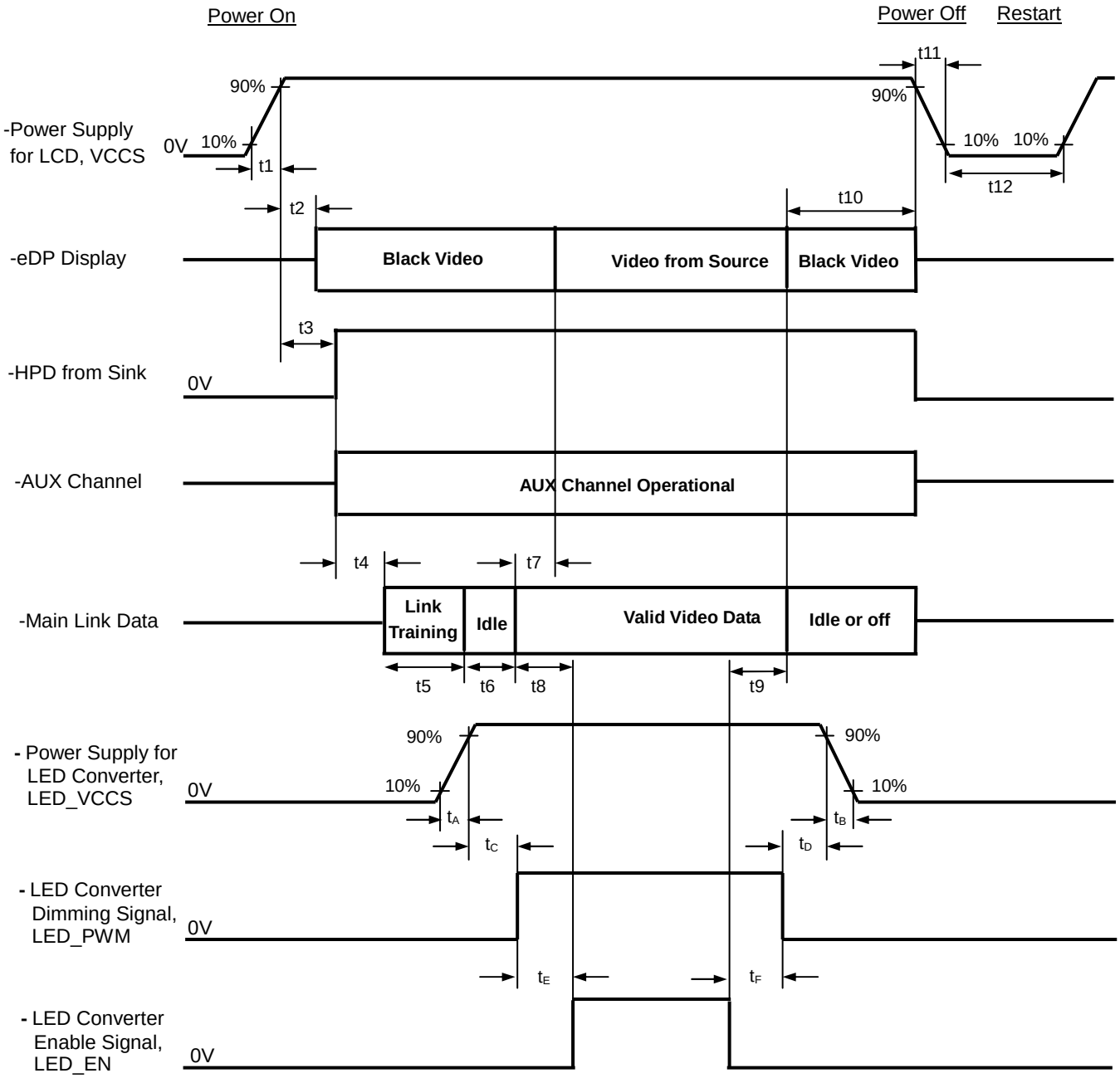
4.6 POWER ON/OFF SEQUENCE



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Timing Specifications: Follow VESA Embedded Display Port Standard Version 1

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	-
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	-
t4	Delay from HPD high to link training initialization	Source	-	-	ms	-
t5	Link training duration	Source	-	-	ms	-
t6	Link idle	Source	-	-	ms	-
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	-
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	-
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	-
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	-
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	10	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	10	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	10	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	10	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

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5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	---	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 5.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° CS-2000T Standard light source "C"	Typ - 0.03	0.664	Typ + 0.03	-	(0),(2),(5),(8)
		Rcy			0.327		-	
	Green	Gcx			0.303		-	
		Gcy			0.592		-	
	Blue	Bcx			0.142		-	
		Bcy			0.087		-	
	White	Wcx			0.332		-	
		Wcy			0.363		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0° CS-2000T, CMO BLU	4.0	4.5			(1),(2),(5),(7),(8)
Contrast Ratio		CR		500	700		-	(2),(3),(8)
Response Time		T_R	θ_x=0°, θ_Y =0°		14	19	ms	(4),(8)
		T_F			11	16	ms	
Transmittance uniformity		δT%	θ_x=0°, θ_Y =0° BM-5A		1.25	1.43	-	(2),(6),(8)
Viewing Angle	Horizontal	θ_x+	CR≥10 BM-5A	80	89			(2),(5),(8)
		θ_x-		80	89			
	Vertical	θ_Y+		80	89			
		θ_Y-		80	89			

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following：

1. Measure Module's and BLU's spectrums. White is without signal input and R, G, B are with signal input. BLU is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (1) Light source is the BLU which is supplied by CMI and driving voltages are based on suitable gamma voltages. White is without signal input and R, G, B are with signal input. Spec is judged by CMI's golden sample.

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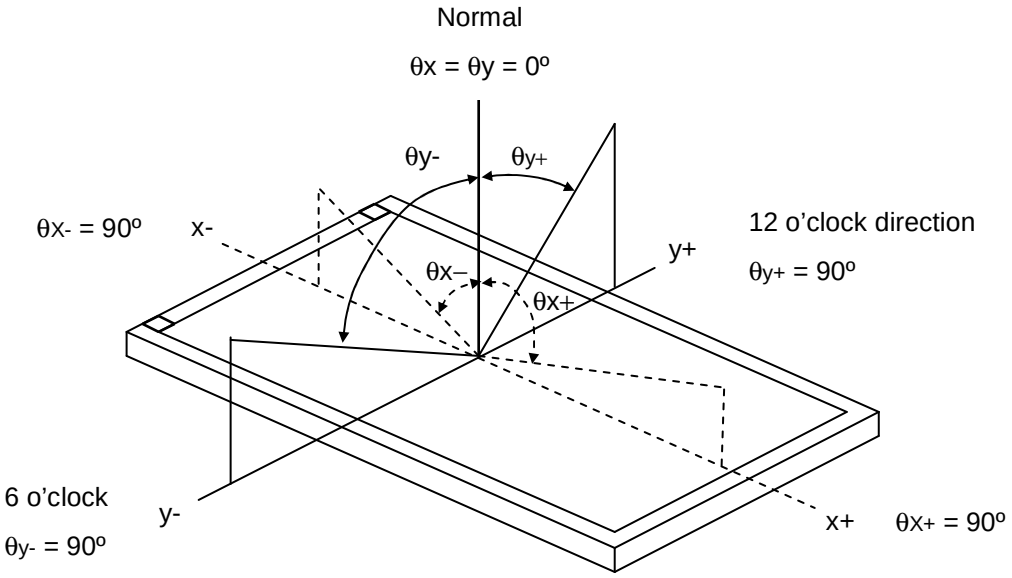
Note (2) Definition of Viewing Angle (θx, θy):



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

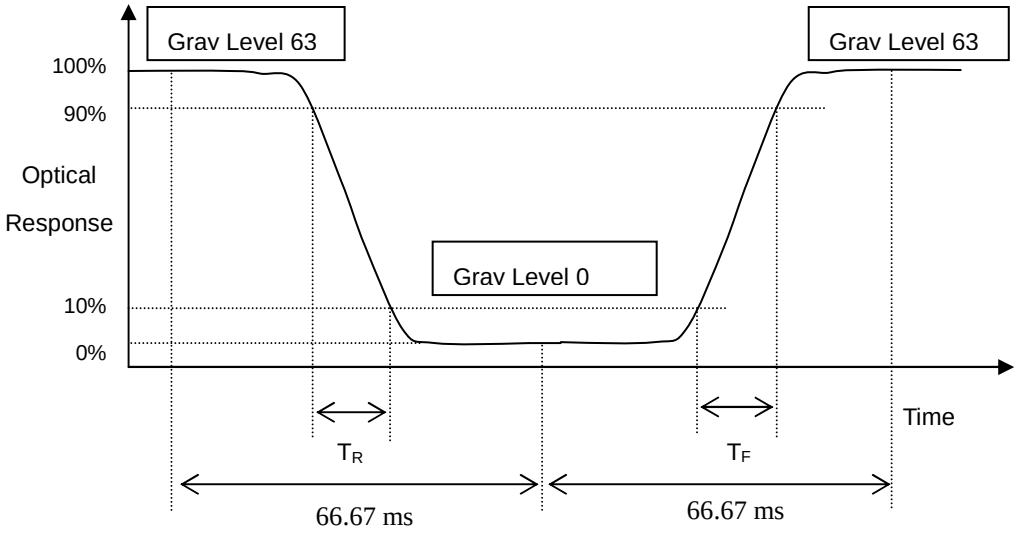
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (4) Definition of Response Time (T_R, T_F):



Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

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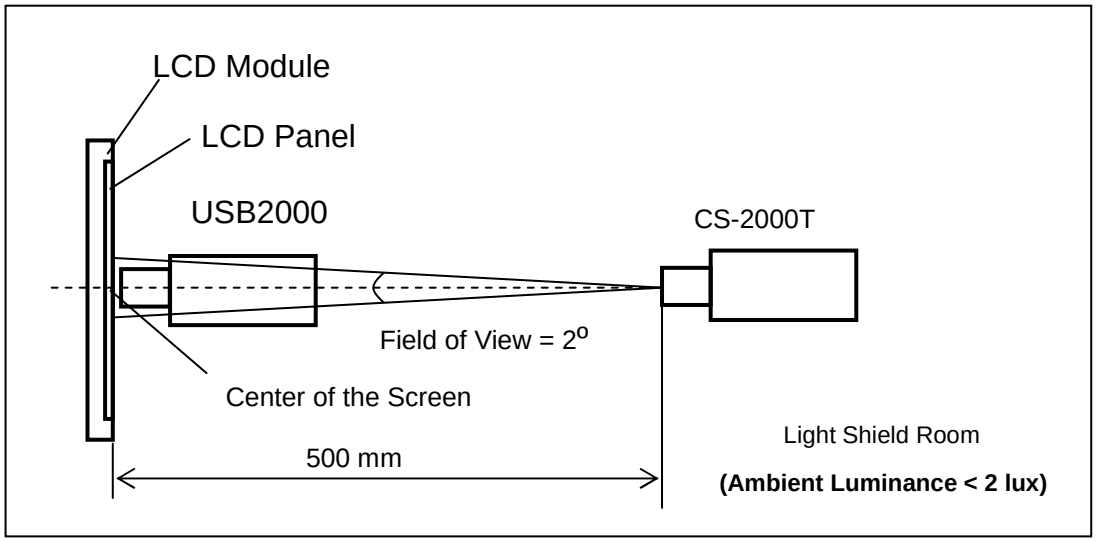


Note (6) Definition of Transmittance Variation (δT%):

Measure the transmittance at 5 points

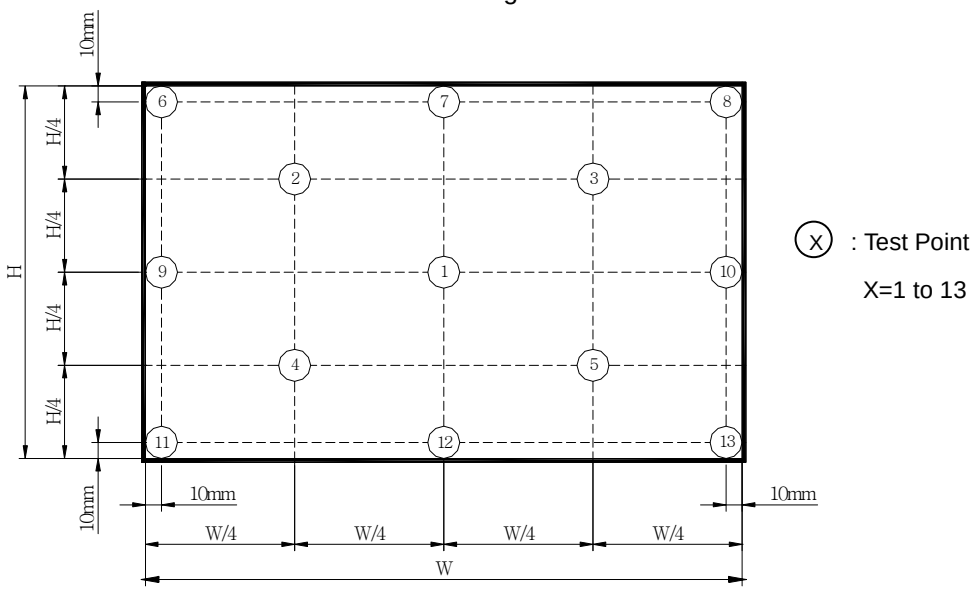
$$\delta T\% = \frac{\text{Maximum [T\%(1), T\%(2), … T\%(5)]}}{\text{Minimum [T\%(1), T\%(2), … T\%(5)]}}$$

Note (7) Definition of Transmittance (T%):

Module is without signal input.

BLU is supplied by CMI.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$



Note (8) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

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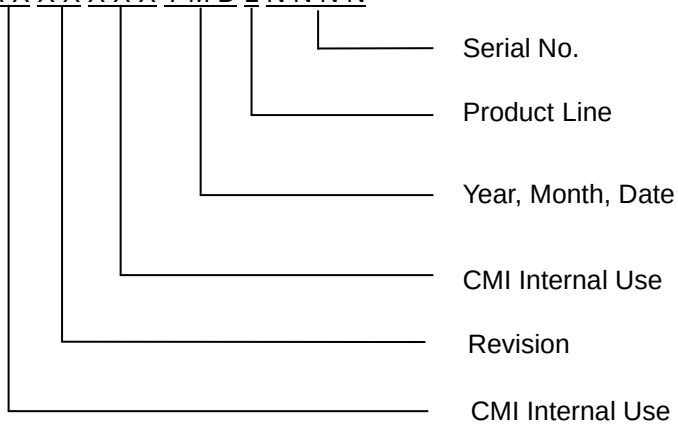
6. PACKING

6.1 CMI OPEN CELL LABEL

The barcode nameplate is pasted on each OPEN CELL as illustration for CMI internal control.

(a) Model Name: N133HSE - DA1

(b) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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6.2 PACKAGE RELIABILITY

(1) Carton Packing should have no failure in the following reliability test items

Test Item	Test Conditions	Note
Packing Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation

6.3 CARTON

(1)Box Dimensions : 540(L)*450(W)*320(H)
(2)40 Modules/Carton

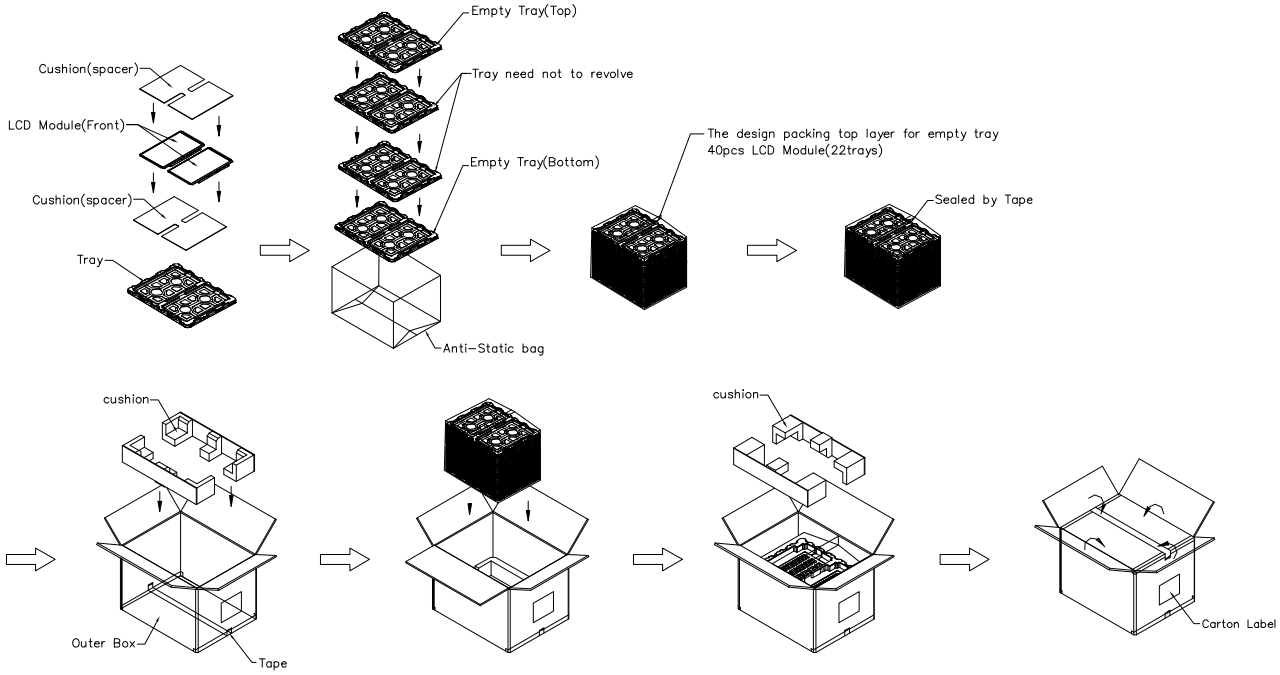

Figure. 6-3 Packing method

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6.4 PALLET

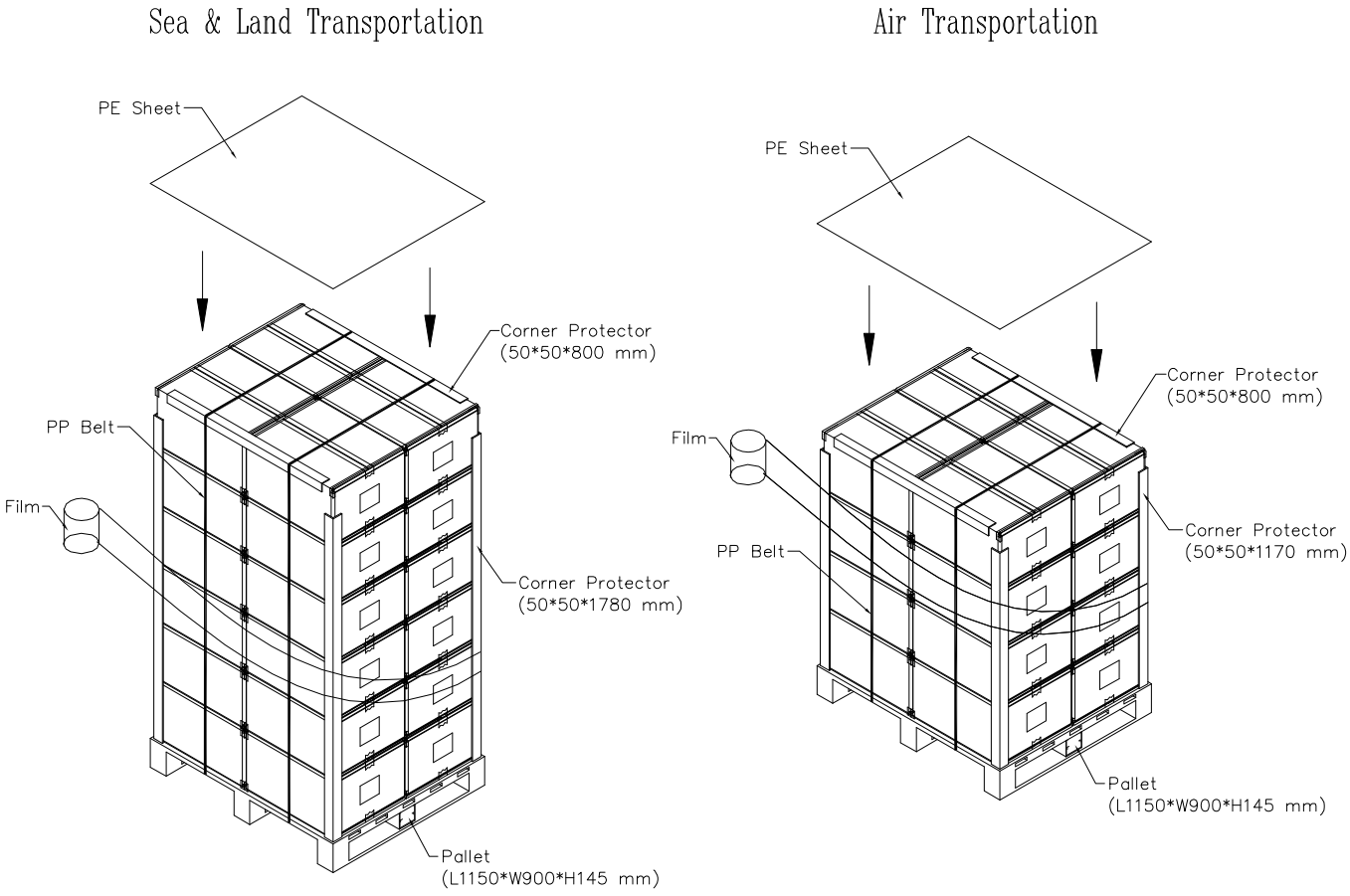

Figure. 6-4 Packing method

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7. PRECAUTIONS

7.1 HANDLING PRECAUTIONS

(1) The open cell should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the open cell.

(2) While assembling or installing open cell, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the open cell from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the open cell.

(10) Pins of I/F connector should not be touched directly with bare hands.

7.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of open cell. Please store open cell within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the open cell, because the moisture may damage open cell when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly.

7.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the open cell is operating.

(2) Always follow the correct power on/off sequence when open cell is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

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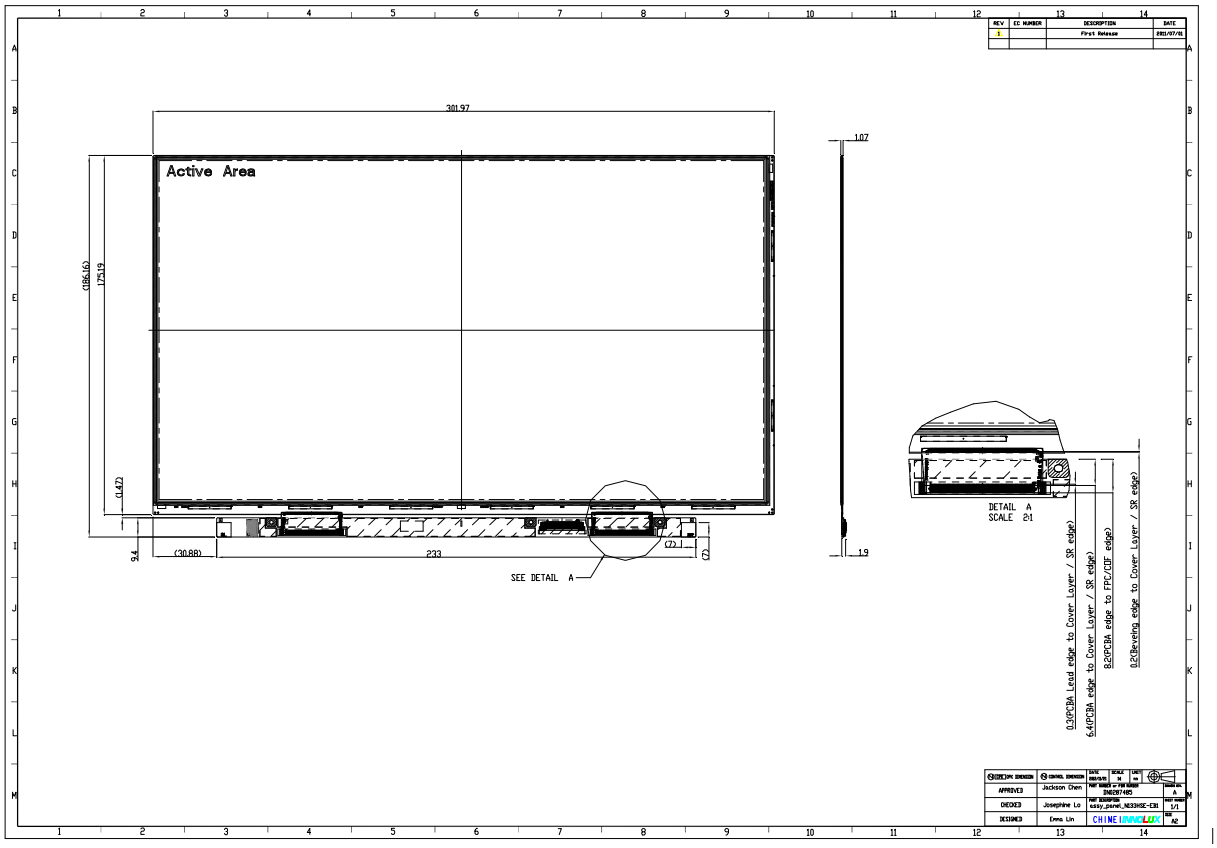
Appendix. OUTLINE DRAWING



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